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AF/2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RICHARD W. ARNOLD ET AL.

Serial No. 09/164,580 (TI-22561)

Filed October 1, 1998

For: KNOWN GOOD DIE USING EXISTING PROCESS INFRASTRUCTURE

Art Unit 2822

Examiner J. Mitchell

Customer No. 23494

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11-18-03

Jay M. Cantor, Reg. No. 19,906

STATUS REQUEST

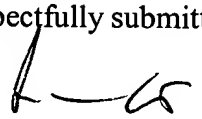
Sir:

Request is hereby made as to the status of the subject application.

A Supplemental Brief on Appeal was filed April 7, 2003, a copy of which is attached hereto along with the PTO mail room acknowledgement of receipt. To date, no response thereto has been received. A review of PAIR does not indicate receipt of this paper. Accordingly, action on the Supplemental Brief on Appeal is believed to be due.

In view of the above, the status of the subject application is requested.

Respectfully submitted,



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Docket number: TI-22561

The following has been received in the United States Patent and Trademark Office on the date stamped:

SUPPLEMENTAL BRIEF ON APPEAL IN TRIPLICATE.

Date: April 7, 2003

Initials: JMC/bhr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

RICHARD W. ARNOLD ET AL.

Serial No. 09/164,580 (TI-22561)

Filed October 1, 1998

For: KNOWN GOOD DIE USING EXISTING PROCESS INFRASTRUCTURE

Art Unit 2822

Examiner J. Mitchell

Commissioner for Patents
Washington, D. C. 20231

Sir:

SUPPLEMENTAL BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

Claims 1 to 4, 9, 10, 13, 14 and 22 to 31 are on appeal and claims 5 to 8 and 17 to 21 have been previously canceled and the appeal as to claims 11, 12, 15 and 16 is hereby withdrawn. Claims 22 to 31 have been copied from Patent No. 6,028,437 for purposes of

interference. Claim 13 is listed to have been rejected, however there is no basis therefore provided in the body of the Office action. Claims 17 to 21 were withdrawn from consideration and are now the subject of a divisional application.

STATUS OF AMENDMENTS

An amendment was filed April 30, 2002 after what was stated in the prior Office action on Form PTO-326 to be a non-final rejection whereas on page 6 of that Office action it is stated that the action is a FINAL rejection. Accordingly, out of an abundance of caution, the amendment filed April 30, 2002 was assumed to be a response to a final rejection. An Advisory Action was received refusing entry of the amendment filed after the alleged final rejection though the only amendment to one claim was one of terminology (correction of an indefinite antecedent) noted by the Examiner in the alleged final rejection. After filing of a Brief on Appeal, prosecution was reopened, resulting in option (2) as stated therein being taken, namely the filing of this Supplemental Brief on Appeal. It is assumed that the unentered amendment filed after final rejection has now been entered in view of the reopening of the prosecution.

SUMMARY OF INVENTION

The invention relates to an apparatus adaptable for the testing of semiconductor devices which includes a package (110 of Fig. 1); and an interconnecting medium (140) contained within the package having electrical paths (171-173) adaptable for coupling to test circuitry. The interconnecting medium (140) includes a medium surface (top surface of 140 in Fig. 1b), a plurality of standoffs (13 of Fig. 3) affixed to the medium surface and a plurality of compliant probe tips (11 of Fig. 3) affixed to the medium surface, the

probe tips being adaptable for making electrical contact with pads on the semiconductor device.

The interconnecting medium or layer for use in a semiconductor package includes an electrically insulating layer (140), electrically conductive paths on the layer (171 to 173), each of he paths having first and second spaced apart regions thereon, the second spaced apart region of each of the paths having a compliant bump (11) having a height greater than all other structures on the layer. A standoff (13) is disposed on the layer and has a height above the layer and less than the bump. The package (110) further includes a package base having an upper surface adapted (base of cavity 112) to receive the interconnecting medium (140), the medium having a medium lower surface (lower surface of 140). A bonding layer (120 and 135), preferably comprised of an elastomeric material, is interposed between the medium lower surface and the package base upper surface and a package lid (160) is provided having a lower surface adapted to receive the semiconductor device, the package lid positioned above the package base. The semiconductor device is a die (130) having an upper surface, the upper surface fixed to the package lid lower surface by a bonding layer interposed therebetween (140 and 150). The semiconductor device is a wafer (130) having an upper surface fixed to the package lid lower surface by a bonding layer interposed therebetween (140 and 150). The bonding layer interposed between the die and the package lid lower surface is comprised of an elastomeric material (page 9, line 11). The compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

ISSUES

1.The issue as to indefiniteness of claims 11, 12, 15 and 16 under 35 U.S.C. 112, second paragraph, is now moot in view of the withdrawal of the appeal of this rejection.

2. Whether claims 1 to 4 are anticipated by Buck et al. (U.S. 5,489,854) under 35 U.S.C. 102(b).

3. Whether claims 9, 10, 14 and 15 are anticipated by Blanton (U.S. 5,220,200) under 35 U.S.C. 102(b).

4. Whether claims 22 to 31 are anticipated by Potter (U.S. 6,028,437) under 35 U.S.C. 102(e).

GROUPING OF CLAIMS

Claims 1 to 4, 9, 10,13 and 14 do not stand or fall together and claims 22 to 31 stand or fall together.

ARGUMENT

ISSUE 1

The issue as to indefiniteness of claims 11, 12, 15 and 16 under 35 U.S.C. 112, second paragraph, is now moot in view of the withdrawal of the appeal of this rejection.

ISSUE 2

Claims 1 to 4 were rejected under 35 U.S.C. 102(b) as being anticipated by Buck et al. The rejection is without merit as will be demonstrated.

Claim 1 requires, among other features, an interconnecting layer having electrically conductive paths thereon disposed in the cavity, each of the paths having first and second spaced apart regions thereon, the first region of each path being aligned with

and contacting a bond pad, the first region including a compliant bump probe tip having a first predetermined height above the layer and further including a standoff on the layer having a second predetermined height above the layer less than the first height. No such structure is taught of even remotely suggested by Buck et al. The alleged interconnecting layer (14) of Buck et al. is clearly stated to be a socket arm, not an interconnect and not having electrically conductive paths thereon. The alleged compliant bump 10 is stated in Buck et al. to be an opening, not a compliant bump.There is no compliant bump probe tip having the claimed height or a standoff as claimed.

Claim 1 further requires an interconnection between said second spaced apart region of each of said paths and one of said plurality of terminals. No such structure is taught or even suggested by Buck et al.

Claims 2 to 4 depend from claim 1 and therefore define patentably over Buck et al. for at least the reasons presented above with reference to claim 1.

In addition claim 2 further limits claim 1 by requiring that the second spaced apart region of each of the paths be a bump aligned with and contacting one of the plurality of terminals. No such feature is taught or suggested by Buck et al. either alone or in the combination as claimed. This combination defines patentably over Buck et al.

Claims 3 and 4 further limit claims 1 and 2 by requiring a compliant layer disposed over the interconnecting layer and providing a force causing engagement of at least the first spaced apart regions and the bond pads. No such feature is taught or suggested by Buck et al. either alone or in the combination as claimed. This combination defines patentably over Buck et al.

ISSUE 3

Claims 9, 10, 14, and 15 (the appeal as to claim 15 has been withdrawn) were rejected under 35 U.S.C. 102(b) as being anticipated by Blanton. The rejection is without merit as will be demonstrated.

Claim 9 requires, among other features, electrically conductive paths on the layer, each having first and second spaced apart regions thereon, the second spaced apart region of each path having a compliant bump having a height greater than all other structures on the layer. No such structure is taught or even suggested by Blanton either alone or in the combination as claimed.

Claim 9 further requires a standoff disposed on the layer and having a height above the layer and less than the bump. No such structure is taught or even suggested by Blanton either alone or in the combination as claimed.

Claims 10 and 14 depend from claim 9 and therefore define patentably over Blanton for at least the reasons presented above with reference to claim 9.

In addition, claim 10 further limits claim 9 by requiring that the second region be a bump extending above the level of the electrically conductive path. No such structure is taught or even suggested by Blanton, either alone or in the combination as claimed. This combination defines patentably over Blanton

Claim 14 further limits claim 10 by requiring that the layer be flexible. No such structure is taught or even suggested by Blanton, either alone or in the combination as claimed. This combination defines patentably over Blanton

ISSUE 4

In a response to an Office action filed November 6, 2001, an amendment was filed amending claims 1 and 9 and adding claims 22 to 31 which were stated to be copied from Potter Patent No. 6,028,437 for purposes of having an interference declared. On pages 6 and 7 of that amendment, it was demonstrated how claim 22 (claim 1 of Potter with altered verbiage as discussed on page 6) was readable on the subject disclosure as well as claim 9. Since interferences are based upon counts rather than claims, it was assumed that this would be sufficient to have an interference declared as long as a prima facie case of invention prior to the filing date of Potter could be established on the record and this was also provided as will be discussed hereinbelow. Any claims that came under the count could be added later on motion if not previously included by this Board.

On November 15, 2001, a Supplement to the Amendment filed November 6, 2001 was filed in which further Declarations, this time signed by the inventors in the subject application, were filed stating that they reduced to practice the invention shown in the attachment to their Declarations prior to May 19, 1997, the filing date of Potter.

In response to these amendments, a final rejection was issued stating that "[a]pplicant (sic) has failed to specifically apply each limitation or element of each of the copied claim(s) to the disclosure of the application". While this requirement was believed to be unnecessary in view of interference practice as discussed above, an amendment was filed April 30, 2002 demonstrating how each of claims 22 to 31 were readable on the subject disclosure. The readability of claims 22 to 31 (the claims copied from the Potter patent) on the subject disclosure is reproduced from the April 30, 2002 amendment as follows in which it was requested that the Declaration filed November 15,

2001, stated to be under 37 C.F.R. 1.131, be treated as being both under 37 C.F.R. 1.608(b) as well as under 37 C.F.R. 1.131 for reasons which will become evident from the arguments presented hereinbelow. It is believed that the Declaration filed November 15, 2001 should have been so treated ab initio. The Declaration filed November 15, 2001 and signed by the inventors clearly establishes evidence which demonstrates that applicants are prima facie entitled to a judgment relative to the patentee. The Declaration and attached evidence which predates the filing date of Patent No. 6,028,437 provides the required explanation particularly stating the basis upon which the applicants are prima facie entitled to the judgment. Clearly, the Declarations of the inventors eliminate Potter as a proper reference in this application under sections 102 or 103 of 35 U.S.C.

[With reference to the rejection of claims 22 to 31 under 35 U.S.C. 102(e), it is apparent that the Potter patent either is or is not available as a reference in this application; it must be one or the other and cannot be both by elementary logic. If it is cited solely in rejection of claims 22 to 31 under 35 U.S.C. 102(e), then the Declarations filed November 6, 2001 and November 15, 2001 under 35 U.S.C. 1.131 remove Potter as a proper reference in this application under that section of the statute. Accordingly, the rejection cannot comply with the requirements of 35 U.S.C. 102(e) since it is based on the Potter patent. On the other hand, if the examiner or this Board is of the opinion, as advanced by applicants and demonstrated in the REMARKS both hereinbelow and in the amendment filed November 6, 2001, that applicants cannot swear back of Potter due to claiming of the same invention as claimed by Potter, then it is incumbent upon the examiner to declare the interference as requested and withdraw the rejection on prior art or for this Board to act sua sponte in declaring an interference. It is readily apparent that

the rejection on Potter on the present record is without merit in any event and this rejection is therefore respectfully traversed for reasons stated above.

In view of the above argument, it is clear that the section of the rejection of claims 22 to 31 is without merit since the Potter reference is disqualified from use as prior art in this application in view of the Declarations filed under 37 C.F.R. 1.131, these Declarations now also having been filed as Declarations under 37 C.F.R. 1.608(b).

With reference to the allegation under Interference on page 2 of the alleged final Office action in paragraph 4, it is respectfully submitted that each limitation of each claim copied for purposes of interference required to provoke an interference in this application has been read on the subject application in the Remarks presented in the amendment. Potter's claims are assumed at this time to be prima facie readable on Potter by the grant of the patent which is presumed to be valid. As long as one claim of Potter is copied and shown to be readable on the subject disclosure, an interference should be declared.

As stated in the amendment filed November 6, 2001 claims 22 to 31 of this application are readable on the Potter patent No. 6,028,437 since they were copied therefrom but for the error noted by the examiner in the final rejection was was refused entry.

Claim 22 is the same as claim 1 of Potter except that the terms used in the subject application "interconnecting medium" have been used in place of the term --probe membrane-- and "medium surface" has been used in place of the term --probe membrane head--. This readability should be sufficient to provide a first count (claim 9 of the subject application can also be used as an additional or alternate count) for purposes of

interference with all other claims coming under the count or counts. Claim 22, which is essentially the same as claim 1 of Potter except as noted above, is therefore readable on the subject disclosure as follows with the bracketed words being those used in Potter:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1); and

an interconnecting medium (140) [probe membrane] contained within said package having electrical paths (171-173) adaptable for coupling to test circuitry, wherein said interconnecting medium [probe membrane] includes a medium surface (top surface of 140 in Fig. 1b) [probe membrane head], a plurality of standoffs (13 of Fig. 3) affixed to said medium surface [probe membrane], and a plurality of probe tips (11 of Fig. 3) affixed to said medium surface [probe membrane head], said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

Claim 9 is readable on Potter as follows:

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer (121 of Potter);

(b) electrically conductive paths on said layer (traces not shown but discussed at column 3, lines 45 to 57), each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump (122) having a height greater than all other structures on said layer; and

(c) a standoff (123) disposed on said layer and having a height above said layer and less than said bump.

With reference to the remaining claims of Potter, these claims would come in under the count, whether or not they can be made in the subject application. Accordingly, the interference should be declared just on the basis of the readability of claims 22 and 9 on the Potter patent. Under the interference Rules, additional claims can be added to come under the count in the Motion period.

With reference to claim 23, this claim is readable on the subject disclosure as follows:

said package (110) further comprising: a package base having an upper surface adapted (base of cavity 112) to receive said interconnecting medium (140), said medium having a medium lower surface (lower surface of 140);

a bonding layer interposed between said medium lower surface and said package base upper surface (120 and 135); and

a package lid (160) having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

With reference to claim 24, the claim is readable on the subject disclosure as follows:

said bonding layer (120 and 135) is comprised of an elastomeric material.

With reference to claim 25, the claim is readable on the subject disclosure as follows:

said semiconductor device is a die (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claim 26, the claim is readable on the subject disclosure as follows:

said semiconductor device is a wafer (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claims 27 and 28, these claims are readable on the subject disclosure as follows:

said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material (page 9, line 11).

With reference to claim 29, this claim is readable on the subject disclosure as follows:

the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

With reference to claim 30, this claim is readable on the subject disclosure as follows:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1), wherein said package has a package lid (160) having a lower surface adapted for receiving said semiconductor device, said semiconductor device (130) having an upper surface, and a package base having an upper surface (112);

an interconnecting medium (140) contained within said package, wherein said interconnecting medium has electrical paths (171, 172, 173) adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips (11) affixed thereto, a plurality of standoffs (13) affixed thereto,

and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads (135) on said semiconductor device (130) and are compliant bump probe tips (sentence bridging pages 9 and 10);

a bonding layer (120, 135) comprising an elastomeric material (page 9, line 11) interposed between said package lid lower surface and said semiconductor device upper surface; and

a bond layer (140, 150) comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.

With reference to claim 31, this claim is readable on the subject disclosure as follows:

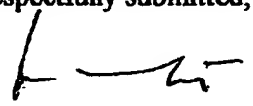
the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

It is believed to be abundantly clear on the record as demonstrated above that appellants have made a prima facie case of not only conception with diligence up to filing of the Provisional Application 60/060,800 from which the subject application claims priority from a date prior to the filing date of Potter, but also to reduction to practice of the invention prior to the filing date of Potter. Accordingly, Potter is not available as a reference in this appeal and all rejections (Issues 1 to 3) are without merit.

CONCLUSION

For the reasons stated above, it is respectfully requested that the final rejection be withdrawn and that the claims on appeal be allowed or that the application be remanded to the examiner for declaration of an interference as originally requested.

Respectfully submitted,



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APPENDIX

The claims on appeal read as follows:

1. An apparatus for testing a semiconductor die which comprises:

(a) a package having a cavity therein;

(b) a plurality of terminals in said package disposed at the periphery of said cavity;

(c) a semiconductor die to be tested having a plurality of bond pads thereon, said die disposed in said cavity;

(d) an interconnecting layer having electrically conductive paths thereon disposed in said cavity, each of said paths having first and second spaced apart regions thereon, said first region of each path being aligned with and contacting a said bond pad, said first region including a compliant bump probe tip having a first predetermined height above said layer and further including a standoff on said layer having a second predetermined height above said layer less than said first height; and

(e) an interconnection between said second spaced apart region of each of said paths and one of said plurality of terminals.

2. The apparatus of claim 1 wherein said second spaced apart region of each of said paths is a bump aligned with and contacting one of said plurality of terminals.

3. The apparatus of claim 1 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

4. The apparatus of claim 2 further including a compliant layer disposed over said interconnecting layer and providing a force causing engagement of at least said first spaced apart regions and said bond pads.

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer;

(b) electrically conductive paths on said layer, each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump having a height greater than all other structures on said layer; and

(c) a standoff disposed on said layer and having a height above said layer and less than said bump.

10. The layer of claim 9 wherein said second region is a bump extending above the level of said electrically conductive path.

13. The layer of claim 9 wherein said layer is flexible.

14. The layer of claim 10 wherein said layer is flexible.

22. An apparatus adaptable for the testing of semiconductor devices comprising:

a package; and

an interconnecting medium contained within said package having electrical paths adaptable for coupling to test circuitry, wherein said interconnecting medium includes a medium surface, a plurality of standoffs affixed to said medium surface, and a plurality of probe tips affixed to said medium surface, said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

23. The apparatus of claim 22, said package further comprising:

a package base having an upper surface adapted to receive said interconnecting medium, said medium having a medium lower surface;

a bonding layer interposed between said medium lower surface and said package base upper surface; and

a package lid having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

24. The apparatus of claim 23, wherein said bonding layer is comprised of an elastomeric material.

25. The apparatus of claim 23, wherein said semiconductor device is a die having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

26. The apparatus of claim 23, wherein said semiconductor device is a wafer having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

27. The apparatus of claim 4, wherein said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material.

28. The apparatus of claim 5, wherein said bonding layer interposed between said wafer and said package lid lower surface is comprised of an elastomeric material.

29. The apparatus of claim 22, wherein the compliant bump probe tips are comprised of a solid material.

30, An apparatus adaptable for the testing of semiconductor devices comprising:

a package, wherein said package has a package lid having a lower surface adapted for receiving said semiconductor device, said semiconductor device having an upper surface, and a package base having an upper surface;

an interconnecting medium contained within said package, wherein said interconnecting medium has electrical paths adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips affixed thereto, a plurality of standoffs affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads on said semiconductor device and are compliant bump probe tips;

a bonding layer comprising an elastomeric material interposed between said package lid lower surface and said semiconductor device upper surface; and

a bond layer comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.

31. The apparatus of claim 30, wherein the compliant bump probe tips are comprised of a solid material.